**MAWLANA BHASHANI SCIENCE AND TECHNOLOGY UNIVERSITY**

SANTOSH, TANGAIL-1902



DEPARTMENT OF INFORMATION AND COMMUNICATION TECHNOLOGY

**Course Title: Digital Logic Design Lab**

**Course Code: ICT-2104**

**Lab Report on:** Implementation of XOR Gate using NAND Gates

**Lab Report No: 04**

|  |  |
| --- | --- |
| Submitted By | Submitted To |
| Name: Kuldip Saha Mugdha  ID: IT22018  2nd Year, 1st Semester  Session: 2021-2022  Dept. of ICT, MBSTU | Dr. Muhammad Shahin Uddin  Professor  DEPARTMENT OF INFORMATION AND COMMUNICATION TECHNOLOGY  MAWLANA BHASHANI SCIENCE AND TECHNOLOGY UNIVERSITY |

**Date of Performance:**

**Date of Submission:**

**Experiment No:** 4

**Experiment Name:** Implementation of XOR Gate using NAND Gates

**Objective:** To implement an XOR (Exclusive OR) gate using only NAND gates and verify its functionality by constructing the circuit and observing the truth table.

**Materials Required:**

* Breadboard
* Power supply (5V DC)
* Connecting wires
* IC 7400 (Quad 2-input NAND gate)
* LEDs (for output visualization)
* Resistors (220Ω)
* Multimeter (optional)

**Procedure:**

**1. Understanding XOR Gate using NAND Gates:**

The XOR gate can be implemented using only NAND gates based on the following Boolean expression:

XOR = (A’B) + (AB’)

- Step 1: Use two NAND gates to invert the inputs A and B.

- Step 2: Create the AND functionality for each term A’B and AB’ using additional NAND gates.

Step 3: Finally, combine the two results using another NAND gate, simulating an OR gate.

**2. Circuit Setup:**

- Place the IC 7400 (Quad 2-input NAND gate) on the breadboard.

- Connect pin 7 to ground and pin 14 to +5V to power the IC.

- Connect the input and output pins as per the logic for constructing the XOR gate using NAND gates. The specific pin connections for the gates are as follows:

- First NAND gate: Inputs A and B.

- Second NAND gate: Connect A and the output of the first NAND gate.

- Third NAND gate: Connect B and the output of the first NAND gate.

- Fourth NAND gate: Use the outputs of the second and third NAND gates as inputs.

- Apply the different combinations of inputs (A and B) and observe the output for each pair.

**3. Verify Output:**

- For each input combination (00, 01, 10, 11), observe the output on an LED connected to the output of the final NAND gate.

- Record the results in the truth table.

**Diagram:**

XOR Gate Implementation using NAND Gates:

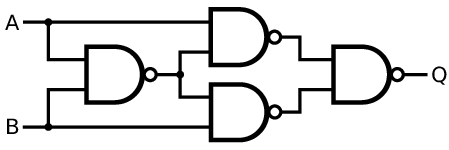


Fig: XOR gate using NAND gate

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| A | B | Q (A ⊕ B) |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Discussion:**

In this experiment, we successfully implemented an XOR gate using only NAND gates, as NAND gates are universal logic gates. The circuit was constructed by combining multiple NAND gates to mimic the XOR function.